IN THE CLAIMS:

Please cancel claims 15, 16, 17, 19 and 20, and amend the claims as follows:

1. (Previously Presented) A flipflop circuit, comprising:

a clock input for applying a clock signal;

a data input for applying a data signal;

an noninverted output;

an inverted output;

a first holding element comprising a first feedback loop comprising a first node and a second node; and

a second holding element comprising a second feedback loop comprising a third node and a fourth node; wherein the first node is coupled to the fourth node via a first signal path and the second node is coupled to the third node via a second signal path exclusive of the first signal path, the second signal path including a delay element in the form of a transmission gate permanently switched on when the circuit is in a normal operating mode;

wherein the first holding element is configured such that at a first clock level of the clock signal the logic value of the data signal is transferred to the first holding element and the logic value of the data signal is made available on the first node, and the inverted logic value of the data signal is made available on the second node; and

wherein the second holding element is configured such that at a second clock level of the clock signal (i) the logic value of the data signal is transferred, and inverted, from the first node to the fourth node, thereby making the inverted logic value of the data signal available on the fourth node, and (ii) the inverted logic value of the data signal is transferred, and inverted, from the second node to the third node, thereby making the noninverted logic value of the data signal available on the third node; wherein the fourth node in the second feedback loop corresponds to the noninverted output and the third node in the second feedback loop corresponds to the inverted output.

2. (Previously Presented) The flipflop of claim 1, wherein at least one of the first and the second feedback loops comprises a negative-feedback inverter circuit formed by two inverting logic elements, wherein an input of each inverter is coupled to an output of the other inverting logic element.

3. (Original) The flipflop of claim 1, further comprising an inverter configured to transfer, and invert, the data signal to the first holding element at the first clock level and further configured to inhibit transfer of the data signal at the second clock level.

4. (Original) The flipflop of claim 1, further comprising a first clock-controlled inverter disposed in the first signal path and a second clock-controlled inverter disposed in the second signal path, wherein each clock-controlled inverter is configured to transfer a respective signal value at the second clock level and inhibit signal value transfer at the first clock level.

5. (Canceled)

6. (Previously Presented) A flipflop circuit, comprising:

a clock input for applying a clock signal;

a data input for applying a data signal;

an noninverted output;

an inverted output;

a first holding element comprising a first feedback loop comprising a first node and a second node;

a second holding element comprising a second feedback loop comprising a third node and a fourth node; wherein the first node is coupled to the fourth node via a first signal path and the second node is coupled to the third node via a second signal path exclusive of the first signal path;

wherein the first holding element is configured such that at a first clock level of the clock signal the logic value of the data signal is transferred to the first holding

element and the logic value of the data signal is made available on the first node, and the inverted logic value of the data signal is made available on the second node;

wherein the second holding element is configured such that at a second clock level of the clock signal (i) the logic value of the data signal is transferred, and inverted, from the first node to the fourth node, thereby making the inverted logic value of the data signal available on the fourth node, and (ii) the inverted logic value of the data signal is transferred, and inverted, from the second node to the third node, thereby making the noninverted logic value of the data signal available on the third node; wherein the fourth node in the second feedback loop corresponds to the noninverted output and the third node in the second feedback loop corresponds to the inverted output;

a reset input configured to receive a reset signal, and wherein the second feedback loop comprises a NOR gate comprising a first input having the reset signal applied thereto; and

wherein the second feedback loop further comprises a NAND gate comprising a first input having an inverted version of the reset signal applied thereto.

7. (Original) The flipflop of claim 6, wherein at least one of the NOR gate and the NAND gate are partially clocked.

8. (Original) The flipflop of claim 7, wherein at least one of the first node and the fourth node and the second node and the third node are coupled via a transmission gate.

9. (Canceled)

10. (Previously Presented) A flipflop circuit, comprising:

a clock input for applying a clock signal;

a data input for applying a data signal;

an noninverted output;

an inverted output;

a first holding element comprising a first feedback loop comprising a first node and a second node;

a second holding element comprising a second feedback loop comprising a third node and a fourth node; wherein the first node is coupled to the fourth node via a first signal path and the second node is coupled to the third node via a second signal path exclusive of the first signal path;

wherein the first holding element is configured such that at a first clock level of the clock signal the logic value of the data signal is transferred to the first holding element and the logic value of the data signal is made available on the first node, and the inverted logic value of the data signal is made available on the second node;

wherein the second holding element is configured such that at a second clock level of the clock signal (i) the logic value of the data signal is transferred, and inverted, from the first node to the fourth node, thereby making the inverted logic value of the data signal available on the fourth node, and (ii) the inverted logic value of the data signal is transferred, and inverted, from the second node to the third node, thereby making the noninverted logic value of the data signal available on the third node; wherein the fourth node in the second feedback loop corresponds to the noninverted output and the third node in the second feedback loop corresponds to the inverted output;

a reset input configured to receive a reset signal, and wherein the second feedback loop comprises a NOR gate comprising a first input having the reset signal applied thereto;

wherein the first feedback loop comprises a NOR gate, so that the second node carries a logic "1" in response to an active state of the reset signal;

wherein the first feedback loop further comprises a decoupling circuit disposed between the first node and the second node and configured to isolate the second node from the third node in the second feedback loop; and

wherein the NOR gate of the first feedback loop is configured to apply a logic "0" to the fourth node in the second feedback loop when the reset signal is in the active state.

11. (Previously Presented) The flipflop of claim 10, wherein the decoupling circuit comprises a transmission gate configured to be switched by the reset signal and an inverter controlled by the reset signal.

12-14. (Canceled)

15. – 17. (Canceled)

18. (Currently Amended) ~~The resettable flipflop circuit of claim 17,~~ A resettable flipflop circuit, comprising:

a single data input;

non-inverted and inverted output nodes for providing non-inverted and inverted logic levels, respectively, of a data signal received via the single data input at a first edge of a clock signal;

a first holding element comprising a first feedback loop with first and second nodes, wherein, on the first edge of the clock signal, the non-inverted and inverted logic levels of the data signal are transferred to the first and second nodes, respectively; and

a second holding element comprising a second feedback loop with third and fourth nodes, wherein, on a second edge of the clock signal, the non-inverted logic level is transferred from the first node to the non-inverted output node via the fourth node and the inverted logic level is transferred from the second node to the inverted output node via the third node;

wherein a propagation delay of the non-inverted logic level from the first node to the non-inverted output node is substantially equal to a propagation delay of the inverted logic level from the second node to the inverted output node and at least the first and second feedback loops each comprise reset circuitry to place the inverted and non-inverted output nodes at known logic levels in response to a reset signal regardless of the state of the clock signal;

wherein the reset circuitry of the second feedback loop comprises one or more gates, each controlled by the clock signal and responsive to the reset signal; and

wherein the one or more gates of the second feedback loop comprise:

a NOR gate with a first input to receive an inverted version of the reset signal, a second input coupled with the fourth node, and an output coupled with the third node; and

a NAND gate with a first input to receive a non-inverted versions of the reset signal, a second input coupled with the third node, and an output coupled with the fourth node of the second input of the NOR gate.

19. – 20. (Canceled)